EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	((simultaneous$3 or parallel$3) near4 (issu$3 or push$3 or deploy$3 or send$3 or us$3) near4 (queue$3 and decod$3)).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:25
L2	3	((simultaneous$3 or parallel$3) with (issu$3 or push$3 or deploy$3 or send$3 or us$3) with (queue$3 and decod$3)).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:25
L3	2	(decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:28
L4	10	(decod$3 with (instruction$1 adj1 queu$3) with parallel).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:28
L5	2	(decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:28
L6	10	(decod$3 with (instruction$1 adj1 queu$3) with parallel).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:29
L7	18	((load$3 or fetch$3) near4 instruction$1 near4 decoder near4 (instruction adj1 queue))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:32
L8	26	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue)))	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:34
L9	1	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue))).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:34
L10	26	(((load$3 or fetch$3) near4 instruction$1) with (decoder near4 (instruction adj1 queue)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:34
L11	122	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:34
L12	9	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue)))	EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:34
L13	13	(((load$3 or fetch$3) with instruction$1) with (decoder with (instruction with queue))).clm.	US-PGPUB; USPAT	OR	OFF	2007/03/19 09:35

EAST Search History

S1	320	(712/219).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:16
S2	407	(712/234).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:16
S3	212	(712/235).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:23
S4	6	decod$3 near4 (instruction$1 adj1 queu$3) near4 parallel	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:26
S5	6	decod$3 near4 (instruction$1 adj1 queu$3) near4 multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:27
S6	14	(decod$3 near4 (instruction$1 adj1 queu$3)) with multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:43
S7	13	(decod$3 near4 (instruction$1 adj1 queu$3)) with parallel	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:42
S8	6	(("5165025") or ("5878254") or ("5958047") or ("6065115") or ("6269439") or ("63816783") or ("6523110")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:40
S9	7	(("5165025") or ("5878254") or ("5958047") or ("6065115") or ("6269439") or ("6381678") or ("6523110")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:40
S10	6	(decod$3 with (instruction$1 adj1 queu$3)) near4 parallel	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:42
S11	0	(decod$3 with (instruction$1 adj1 queu$3)) near4 multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:43
S12	62	(decod$3 with (instruction$1 adj1 queu$3)) with instruction$1 with load$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 14:43

EAST Search History

S13	25	(decod$3 near4 (instruction$1 adj1 queu$3)) with instruction$1 with load$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 15:43
S14	20	branch$3 near4 decod$3 near4 (bypass$3 or skip$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 15:50
S15	15	(branch$3 near4 decod$3 near4 stag$3) with (instruction near4 queu$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:00
S16	10	(pre?decod$3 near4 stag$3) with (instruction near4 queu$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:01
S17	335	(711/138).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:26
S18	91	(cach$3 near4 fill$3) near4 (bypass$3 or skip$4 or forward$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:33
S19	13	(cach$3 near4 fill$3) near4 (instruction$1 near4 forward$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/09/28 16:33
S20	217	(712/235).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:03
S21	413	(712/234).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:03
S22	333	(712/219).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:03
S23	343	(711/138).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:04
S24	1195	(empty or initializ$5 or start$3 or begin$5) near4 (queue$3 or buffer$3) near4 decod$4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:07

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S25	12	(empty or initializ$5 or start$3 or begin$5) near4 (queue$3 or buffer$3) near4 decod$4 near4 fetch$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:12
S26	0	(invalid adj1 data) near4 (queue$3 or buffer$3) near4 decod$4 near4 fetch$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:12
S27	3	(instruction$1 adj1 queu$3) near4 (decod$3) near4 (simultaneous$3 or parallel$3) near4 (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:15
S28	4	((instruction$1 adj1 queu$3) near4 (decod$3)) with ((simultaneous$3 or parallel$3) near4 (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:17
S29	6	((instruction$1 adj1 queu$3) near4 (decod$3)) same ((simultaneous$3 or parallel$3) near4 (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:20
S30	15	((instruction$1 adj1 queu$3) near4 (decod$3)) same ((simultaneous$3 or parallel$3) with (fetch$3 or insert$3 or add$3 or push$3 or enqueu$5))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:28
S31	11	mispredict$5 with (decod$3 with (instruction$1 near4 queu$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:31
S32	44	mispredict$5 same (decod$3 with (instruction$1 near4 queu$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/10 21:31
S33	2	(simultaneous$3 or parallel$3) near4 load$3 near4 (queue$3 and decod$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/12 14:41
S34	1	(simultaneous$3 or parallel$3) near4 insert$3 near4 (queue$3 and decod$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/12 14:42
S35	4	(simultaneous$3 or parallel$3) near4 (issu$3 or push$3 or deploy$3 or send$3 or us$3) near4 (queue$3 and decod$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/19 09:23

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S36	15	(decod$3 near4 (instruction$1 adj1 queu$3)) with multiplex$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 14:50
S37	3	(trac$3 near4 buffer$3) near4 (decod$3 near4 (multiplex$4 or select$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 14:51
S38	47	(trac$3 near4 buffer$3) with (decod$3 near4 (multiplex$4 or select$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 14:58
S39	7	(trace near4 buffer$3) same (decod$3 near4 (multiplex$4 or select$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:01
S40	0	(trace near4 buffer$3) near4 (decod$3) near4 (parallel or simultaneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:01
S41	3	(trace near4 buffer$3) with (decod$3) with (parallel or simultaneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:03
S42	38	(trace) with (decod$3) with (parallel or simultaneous$2)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:03
S43	10	(trace) with (decod$3) with (parallel or simultaneous$2) with (load$3 or execut$3 or operat$3 or stor$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:07
S44	286	(trace) with (decod$3) with (instruction$1)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:07
S45	129	(trace) with (decod$3) with (instruction$1) with cach$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:07
S46	95	(trace) with (decod$3) with (instruction$1 near4 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:08
S47	93	(trace near4 (buffer$1 or memor$3 or cach$3)) with (decod$3) with (instruction$1 near4 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/15 15:08

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(parallel or simultaneous) + decoder + "instru [Search] Advanced Scholar Search | Scholar Preferences | Scholar Help

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Scholar All articles | Recent articles Results 1 - 10 of about 436 for (parallel or simultaneous) + decoder + "instruction queue". (0.16 seconds)

All Results
J Lo
D Tullsen
S Eggers
J Emer
H Levy

Exploiting choice: instruction fetch and issue on an implementable **simultaneous** multithreading ... - group of 51 »
DM Tullsen, SJ Eggers, JS Emer, HM Levy, JL Lo, RL ... - Proceedings of the 23rd annual international symposium on ..., 1996 - portal.acm.org
... of a wide-issue processor without **simultaneous** multithreading. ... by the peak fetch and **decode** bandwidths, which ... our architecture more than a **parallel** program by ...
Cited by 484 - Related Articles - Web Search - BL Direct

An Elementary Processor Architecture with **Simultaneous** Instruction Issuing from Multiple Threads - group of 5 »
H Hirata, K Kimura, S Nagamine, Y Mochizuki, A ... - Computer Architecture, 1992. Proceedings., The 19th Annual ..., 1992 - ieeexplore.ieee.org
... Elementary Processor Architecture with **Simultaneous** Instruction Issuing ... chitectural interest upon **parallel** multithreading and ... **queue** unit and **decode** unit pairs ...
Cited by 138 - Related Articles - Web Search - BL Direct

Converting Thread-Level Parallelism to Instruction-Level Parallelism via **Simultaneous** Multithreading - group of 28 »
JL LO, SJ EGGERS, JS EMER, HM LEVY, RL STAMM, DM ... - ACM Transactions on Computer Systems, 1997 - portal.acm.org
... Following instruction fetch and **decode**, register renaming is performed ... shallow is from the Applied **Parallel** Research HPF ... **Simultaneous** Multithreading • 331 ...
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Initial observations of the **simultaneous** multithreading Pentium 4 processor - group of 12 »
N Tuck, DM Tullsen - **Parallel** Architectures and Compilation Techniques, 2003. ... - ieeexplore.ieee.org
... trace cache and main instruction **decoder** are handled in ... when two threads ran **simultaneous** copies of ... 12th International Conference on **Parallel** Architectures and ...
Cited by 39 - Related Articles - Web Search

A MULTITHREADED ARCHITECTURE APPROACH TO **PARALLEL** DSPs FOR HIGH PERFORMANCE IMAGE PROCESSING ...
JP Wittenburg, P Pirsch, G Meyer - ieeexplore.ieee.org
... an architec- ture's resources (**simultaneous** multithreading ... DSP specific extensions Though data **parallel** loops can ... the name, the following **Decode & Instruction** ...
Cited by 7 - Related Articles - Web Search

Speculative **instruction queue** and method therefor particularly suitable for variable byte-length ... - group of 3 »
DB Witt... - US Patent 5,826,053, 1998 - Google Patents
... [il] Patent Number: [45] Date of Patent: [54] SPECULATIVE **INSTRUCTION QUEUE** AND METHOD THEREFOR PARTICULARLY SUITABLE FOR VARIABLE BYTE-LENGTH INSTRUCTIONS ...
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Pipeline control for a single cycle VLSI implementation of acomplex instruction set computer
DR Stiles, HL McFarland, NG Microsyst, CA San Jose - COMPCON Spring'89. Thirty-Fourth IEEE Computer Society ... - ieeexplore.ieee.org
... prefetch of up to three **simultaneous** instruction streams. ... Instruction **decode** generally proceeds at a single cycle rate. ... allows IEU to perform **parallel** and/or ...
Cited by 12 - Related Articles - Web Search

Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction ... - group of 6 »
JG Favor, K Van Dyke, DR Stiles - US Patent 5,226,130, 1993 - Google Patents
... 'In **parallel** with the fetching and/or decoding of a branch instruction, the instruction is also looked up in the branch prediction cache. ...
Cited by 234 - Related Articles - Web Search

Parallel processing unit which processes branch instructions without decreased performance when a ... - group of 3 »
H Ando - US Patent 5,809,294, 1998 - Google Patents
... [il] Patent Number: [45] Date of Patent: [54] **PARALLEL** PROCESSING UNIT WHICH PROCESSES BRANCH INSTRUCTIONS WITHOUT DECREASED PERFORMANCE WHEN A BRANCH IS TAKEN ...
Cited by 15 - Related Articles - Web Search

Improving CISC instruction decoding performance using a fill unit - group of 6 »
M Smotherman, M Franklin - Proceedings of the 28th annual international symposium on ..., 1995 - portal.acm.org
... only the first instruction in the **instruction queue** can produce ... Figure 4: **Simultaneous**, triple-instruction-**decode** microoperations using P6-like **decoder**, ...
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All Results

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J Lo
S Eggers
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H Levy

... cache memory line as either branch target entry or prefetch **instruction queue** based upon instruction ... - group of 5 »
KS Van Dyke, DR Stiles, JG Favor... - US Patent 5,748,932, 1998 - Google Patents
... By doing this in **parallel** with the ... ofthe ETC to serve as instruction queues, into an **instruction queue** from which the ... **decoder's** instruction register is loaded. ...
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The approach to multiple instruction execution in the GMICRO/400processor
T Yoshida, M Matsuo, S Iwata - TRON Project Symposium, 1991. Proceedings., Eighth, 1991 - ieeexplore.ieee.org
... branch instruction, and the other **instruction queue** holds the ... The superscalar instruction **decode** unit decodes two instructions in **parallel** if the two ...
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Apparatus for concurrent multiple instruction decode in variable length instruction set computer - group of 2 »
CM Chuang - US Patent 5,371,864, 1994 - Google Patents
... group oftwo or more instructions in **parallel**, the start- ... **Instruction queue** 56 may, for exam- ... **decoder** for the instruction set ofthe Intel 80386 (trade- ...
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Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading ... - group of 51 »
DM Tullsen, SJ Eggers, JS Emer, HM Levy, JL Lo, RL ... - Proceedings of the 23rd annual international symposium on ..., 1996 - portal.acm.org
... bounded by the peak fetch and **decode** bandwidths, which ... assume a 32-entry integer **instruction queue** (which han- ... our architecture more than a **parallel** program by ...
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Microprocessor having precoder unit and main **decoder** unit operating in pipeline processing manner - group of 2 »
N Suzuki - US Patent 5,233,696, 1993 - Google Patents
... contents ofBFF 140 are supplied to a main **decoder** unit (MDU ... MMU 170 and EXU ISO, operate in **parallel** in a ... INSQ3) 121-1 to 121-4 ofan **instruction queue** 121, each ...
Cited by 51 - Related Articles - Web Search

... performance superscalar microprocessor including a speculative **instruction queue** for byte-aligning ... - group of 3 »
DB Witt, WM Johnson... - US Patent 5,751,981, 1998 - Google Patents
... 29m 1993 entitled "Speculative **Instruction Queue** and Method Therefor Particularly Suitable ... 29, 1993 entitled "Superscalar Instruction **Decoder**"—David B. Witt ...
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Data processing system with **instruction queue** having tags indicating outstanding data status - group of 2 »
TN Hicks, MH NguyenPhu - US Patent 5,150,470, 1992 - Google Patents
... 35 embodiment includes the capability to **decode** multiple many ... instructions in **parallel**. The load instructions are stored in an **instruction queue** (the memory to ...
Cited by 17 - Related Articles - Web Search

Method for refilling **instruction queue** by reading predetermined number of instruction words ... - group of 2 »
US Patent 5,317,701, 1994 - freepatentsonline.com
... Wharton, "**Parallel** 486 Pipelines Produce Peak Processor Performance ... word set from the **instruction queue** 50 ... third instruction cycle, prefetch **decoder** 56 advances ...
Cited by 26 - Related Articles - Cached - Web Search

... data processing system with decoding and execution of prefetched instructions in **parallel** - group of 3 »
H Yamahata, Y Sato - US Patent 4,847,748, 1989 - Google Patents
... When the queue is the decoded **instruction queue** memory advances, the ... The in- struction

decode unit can execute the ... decod- ing and execution in **parallel**, and a ...
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Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction ... - group of 6 »
JG Favor, K Van Dyke, DR Stiles - US Patent 5,226,130, 1993 - Google Patents
... 'In **parallel** with the fetching and/or decoding of a branch instruction, the instruction is also looked up in the branch prediction cache. ...
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All Results

D Tullsen
J Emer
J Lo
S Eggers
H Levy

Exploiting choice: instruction fetch and issue on an implementable simultaneous multithreading ... - group of 51 »
DM Tullsen, SJ Eggers, JS Emer, HM Levy, JL Lo, RL ... - Proceedings of the 23rd annual international symposium on ..., 1996 - portal.acm.org
... than suffer this penalty, we schedule load-dependent instructions ... is bounded by the peak fetch and decode ... assume a 32-entry integer instruction queue (which han ...
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POWER4 system microarchitecture - group of 13 »
JM Tendler, JS Dodson, JS Fields Jr, H Le, B ... - IBM Journal of Research and Development, 2002 - research.ibm.com
... GD cycles are the cycles during which instruction decode and group ... a result of a processor L1 data-cache load request or instruction-fetch request that ...
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An Elementary Processor Architecture with Simultaneous Instruction Issuing from Multiple Threads - group of 5 »
H Hirata, K Kimura, S Nagamine, Y Mochizuki, A ... - Computer Architecture, 1992. Proceedings., The 19th Annual ..., 1992 - ieeexplore.ieee.org
... In such a case, another cache and fetch unit would be needed. ... The instruction set is based on a RISC type, and a load/store architecture is assumed. ...
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The case for a single-chip multiprocessor - group of 37 »
K Olukotun, BA Nayfeh, L Hammond, K Wilson, K ... - ACM SIGPLAN Notices, 1996 - portal.acm.org
... eg integer, floating point, load/store ... Three factors constrain instruction fetch: mispredicted branches, instruction mis ... align a packet of instructions for the ...
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A dynamic multithreading processor - group of 25 »
H Akkary, MA Driscoll - Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ... - ieeexplore.ieee.org
... a misprediction is detected from either source, instruction fetch is switched ... Instructions Mappings & Operands to Rename Unit From Load Queue ... Instruction Queue ...
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Data processing system with instruction queue having tags indicating outstanding data status - group of 2 »
TN Hicks, MH NguyenPhu - US Patent 5,150,470, 1992 - Google Patents
... PRE-FETCH BUFFER CONTROL ... loaded as a result ofa load instruction, the float- ing point :.. instruction decode logic interconnected to the instruction queue in the ...
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... performance superscalar microprocessor including a speculative instruction queue for byte-aligning ... - group of 3 »
DB Witt, WM Johnson... - US Patent 5,751,981, 1998 - Google Patents
... also share a common reorder buffer, register file, branch prediction unit and load/ store unit ... INSTRUCTION DECODER ... FETCH PC, MISPREDICT STATUS SPEC.BRANCH BUS ...
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Paired instruction processor precise exception handling mechanism - group of 2 »
RL Jardine, SJ Lynch, PR Manela, RW Horst - US Patent 5,075,844, 1991 - Google Patents
... O * OA, LOAD CIF ... 1, a fetch unit (FU) 10 is coupled to an in -struction cache (1C) 12 ... and ROF) 18 and 20 are connected ini series to form an instruction queue 21 ...
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Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length ... - group of 5 »
DB Witt, MD Goddard... - US Patent 5,689,672, 1997 - Google Patents
... to four instructions into a sequence of one or more internal RISC-like operations (ROPs), and the parallel dispatch of up to 4 ROPs by an instruction decoder. ...
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Multiple instruction issue in the NonStop cyclone processor - group of 3 »
RW Horst, RL Harris, RL Jardine - ACM SIGARCH Computer Architecture News, 1990 - portal.acm.org
... to register move, LOAD1 = load indirect. 218 ... Fetch instructions INSTRUCTION and predict ADDRESS branches REGISTERS PED INSTRUCTION CACHE S = Second F = First ...
Cited by 34 - Related Articles - Web Search

(load or fetch) + instruction + deco Search

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